UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,161	10/14/2003	Carl A. Bender	POU920030202US1	4774

7590 11/19/2007

Lawrence D. Cutter, Attorney
IBM Corporation, Intellectual Property Law Dept.
M/S P386
2455 South Rd.
Poughkeepsie, NY 12601

EXAMINER	
KASRAIAN, ALLAHYAR	
ART UNIT	**PAPER NUMBER**
2617	
MAIL DATE	**DELIVERY MODE**
11/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	**Application No.** 10/685,161	**Applicant(s)** BENDER ET AL.	
	Examiner Allahyar Kasraian	**Art Unit** 2617	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7,8 and 11-17* is/are rejected.

7)☒ Claim(s) *4,5,9,10 and 18-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Art Unit - Location

1. The Art Unit location of this application in the USPTO has changed. To aid in correlating any papers for this application, all further correspondence regarding this application should be directed to Art Unit 2617.

Continued Examination Under 37 CFR 1.114

2. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

2. **Claims 5 and 6** objected to because of the following informalities:
   a. **Claim 5** depends on claim 3 that has no limitation with regards to "a channel or channels. Examiner assumes **claim 5** should depend on **claim 4** since the further limitation of "said channel" should be from the indication of "a channel" in claim 4.
   b. **Claim 6** depends on claim 3 that has no limitation with regards to "a channel or channels. Examiner assumes **claim 5** should depend on **claim 4** since the further limitation of "said channel" should be from the indication of "a channel" in claim 4.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. **Claims 11-13** rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Consider **claim 11 as applied to claim 7**, there is no support in the specification with respect to “fencing mechanism”.

Claims 12 and13 are rejected based on their virtue of dependency.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless – (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. **Claims 14-17** are rejected under 35 U.S.C. 102(a) as being anticipated by **Pettey et al. (U.S. Patent # 6,594,712 B1)** (hereafter Pettey).

Consider **claim 14**, Pettey clearly shows and discloses a method for the communication of message packets from a first node in a data processing system to a plurality of nodes in said data processing system, said method comprising the steps of:

establishing a first set of communication parameters, prior to message packet transmission time, in a communications adapter connected to said first node, said first set of communication parameters including an indication that a plurality of nodes is targeted for receipt of said message packet, said first set of communication parameters also including a destination identifier (see FIG. 9, FIG. 2 and lines 27-30 of col. 12, "a plurality of local address fields 912 to 918 for specifying addresses on the PCI buses 212 and 216 of FIG. 2."; and Lines 25 of col. 14, for utilizing SGLs 900 to generate the transmit packet by TxPP logic 1414 of FIG. 14)

establishing a second set of communication parameters, prior to message transmission time in communication adapters connected to said plurality of nodes, said second set of communication parameters including an entry which maps said destination identifier to an address in memory at said plurality of nodes (see lines 43-45 for utilizing SGLs 900 of FIG. 9 by RxPP logic 1416 of FIG. 14, "The RxPP logic 1416 also utilizes SGLs 900 of FIG. 9 to transfer data in a received packet to local addresses on the PCI buses 212 and 216." See FIG. 5 for mapping memory and lines 45-49 of col. 14, "If the received packet is an RDMA ...then the local PCI addresses will be specified in the DRDMA Address Space 508 of FIG. 5.");

transmitting a message packet, with header information linking said packet to said first and second set of communication parameters, from said adapter connected to said plurality of nodes, using said first set of communication parameters (see FIG. 1 for nodes 102, FIG. 4 for PMB packet with header which includes IB that carry SGL parameters described in lines 2-4 of col. 8, lines 64-67 of col. 8, lines 32-34 of col. 11 and line 13 of col. 12) ;

recognizing, at adapters connected to said respective ones of said plurality of nodes, which receive message packets from said adapter connected to said first node, that said message packet is targeted for receipt by a plurality of nodes, whereby data in said packet is transferred directly from memory locations in said first node directly to memory locations in memory at said plurality of nodes (see lines 40-43 of col. 14 "The Bus Router 306 also includes Receive Packet Process (RxPP) logic 1416 for processing incoming IB packets such as those of FIGS. 10 to 13 received from an IB source node, such as host 102 of FIG. 1"); and

transmitting a message packet with header information linking said packet to a first and second set of communication parameters, whereby data in said packet is transferred directly from memory locations associated with one node directly to memory locations associated with another node (see lines 28-30 of col. 1 for a direct memory accessing, "One feature of the IBA that facilitates high-speed data transfers is the Remote Direct Memory Access (RDMA) operation."; and lines 2-4 of col. 8 for creating IB packet headers; and FIG. 4 for format of a Packet Memory Block (PMB) and lines 64-67 of col. 8 for linking IB parameters in the PMB packets; IB are created for WQE which includes SGL as described in lines 32-34 of col. 11 and line 13 of col. 12).

Consider **claim 15 as applied to claim 14 above**, Pettey clearly shows and discloses a plurality of channels is provided and associated with one or a plurality of nodes (see FIG. 2 for IB I/O Units and I/O devices and definition of IB channel Adapter in lines 54-62 of column 1, "A Channel Adapter connects a bus within the IB node that is capable of accessing the IB node memory, such as a PCI bus, processor bus or memory bus, with the IB network. In the case of an IB I/O node, the CA also connects I/O devices such as disk drives or network interface devices, or the I/O controllers connected to the I/O devices, with the IB network. A CA on an IB I/O node is commonly referred to as a Target Channel Adapter (TCA) and an IB processor node is commonly referred to as a Host Channel Adapter (HCA).")

Consider **claim 16 as applied to claim 15 above**, Pettey clearly shows and discloses one or more tasks can be associated with each of said channels (in is inehernetly taught since every IB I/O node or PCU bus or memory has different functionality therefore, their IB channel has assigned different tasks).

Consider **claim 17 as applied to claim 14 above**, Pettey clearly shows and discloses at least one channel is provided, said channel being associated with at least one node and one task (lines 8-14 of abstract, "the channel adapter receives the data into an internal buffer and creates an Infiniband RDMA Write packet for transmission to virtual address within a remote Infiniband node.")

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the Examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the Examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. **Claims 1 and 3** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Pettey et al. (U.S. Patent # 6,594,712 B1)** (hereafter Pettey) in view of **Yasuda et al. (U.S. Patent # 6,338,095 B1)** (hereafter Yasuda).

Consider **claim 1**, Pettey clearly shows and discloses a method for the communication of message packets between nodes in a data processing system, said method comprising the steps of:

establishing a first set of communication parameters prior to message transmission time in a communications adapter connected to a first one of said nodes, said first set of communication parameters including a destination identifier (see FIG. 9, FIG. 2 and lines 27-30 of col. 12, "a plurality of local address fields 912 to 918 for specifying addresses on the PCI buses 212 and 216 of FIG. 2." See FIG. 8 and lines 13-23 of col. 12 "The WQE 800 also includes a SGL local address field 812 for specifying the physical address in local memory 218 of a scatter/gather list (SGL), described below with respect to FIG. 9... The WQE 800 also includes other fields 816 for specifying information necessary... destination local ID, destination global ID..." and Lines 25 of col. 14, for utilizing SGLs 900 to generate the transmit packet by TxPP logic 1414 of FIG. 14);

establishing a second set of communication parameters prior to message transmission time in a communications adapter connected to a second one of said nodes, said second set of communication parameters including an entry which maps said destination identifier to an address in memory in said second node (see lines 43-45 for utilizing SGLs 900 of FIG. 9 by RxPP logic 1416 of FIG. 14, "The RxPP logic 1416 also utilizes SGLs 900 of FIG. 9 to transfer data in a received packet to local addresses on the PCI buses 212 and 216." See FIG. 5 for mapping memory and lines 45-49 of col. 14, "If the received packet is an RDMA ... then the local PCI addresses will be specified in the DRDMA Address Space 508 of FIG. 5.");

transmitting a message packet with header information linking said packet to said first and second set of communication parameters, whereby data in said packet is transferred directly from memory locations in said first node directly to memory locations in memory at said second node (see lines 28-30 of col. 1 for a direct memory accessing, "One feature of the IBA that facilitates high-speed data transfers is the Remote Direct Memory Access (RDMA) operation."; and lines 2-4 of col. 8 for creating IB packet headers; and FIG. 4 for format of a Packet Memory Block (PMB) and lines 64-67 of col. 8 for linking IB parameters in the PMB packets; IB are created for WQE which includes SGL as described in lines 32-34 of col. 11 and line 13 of col. 12);

However, Pettey fails to explicitly disclose assembling packet headers in a communications adapter, by executing at least one script command stored in memory within said adapter to gather header information within an internal adapter buffer; and executing at least one other script command stored in memory within said adapter to form completed packet headers from information gathered into said internal buffer.

In the same field of endeavor, Yasuda disclose assembling packet headers in a communications adapter, by executing at least one script command stored in memory within said adapter to gather header information within an internal adapter buffer (see FIG. 4, MESSAGE SEND CIRCUIT 408, COMMAND SEND CIRCUIT 411, COMMAND PROCESSOR CIRCUIT 406, and in FIG. 3 for INSTRUCTION PROCESSOR 301, and lines 11-13 of column 11; lines 17-24 of column 9 for executing program processes; and FIG. 2 TRANSFER CONTROL INFORMATION 200, and lines 50-52 for the header of the message information within the transfer control);

and executing at least one other script command stored in memory within said adapter to form completed packet headers from information gathered into said internal buffer (see lines 48-68 of column 13, where it says, “The message assembly circuit 513 assembles a message having structure decided according to the value of the mode bit and sends a send request of the message to the message send circuit 408. When the mode bit is one, the selector 514 assembles a message which contains a header which contains part of the transfer control information 200 read from the local memory 304 and sent via the command processing circuit 406, and a data portion which contains the user data and the MPI additional information, and sets the assembled message into the register 515.”)

Therefore it would have been obvious to a person or ordinary skills in the art at the time the invention was made to incorporate the header assembler as taught by Yasuda to the I/O controller disclosed by Pettey for purpose of making headers for exchanging messages with the interconnecting network. The proper motivation is to building control headers message to direct and process information data.

Consider **claim 3**, Pettey as modified by Yasuda disclosed the claimed invention **as applied to claim 1 above**, in addition Pettey discloses the step of processing said packet such that when said package arrives, it is assigned to a task (see lines 34-36 of col. 7, "The IB MACs 308 perform buffering… and other physical and link layer management tasks.").

Consider **claim 4**, Pettey as modified by Yasuda disclosed the claimed invention **as applied to claim 3 above**, in addition Pettey discloses the step of assigning each task to a channel based upon packet headers (see lines 54-62 of column 1 for definition of IB Channel adapter and an IB packet is header for the PMB packet shown in FIG. 4 and has different task for each I/O node)s

8. **Claim 2** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Pettey et al. (U.S. Patent # 6,594,712 B1)** (hereafter Pettey) in view of **Yasuda et al. (U.S. Patent # 6,338,095 B1)** (hereafter Yasuda) further in view of **Anderson (U.S.**

Patent # 6,931,003 B2) and further in view of **Ise et al. (U.S. Patent # 6,643,258 B1)** (hereafter Ise).

Consider **claim 2 as applied to claim 1 above**, Pettey as modified by Yasuda disclose the claimed invention except prioritizing messages based on their intended destination such that tasks received by different nodes can be processed simultaneously; and prioritizing messages intended for same nodes chronologically such that they can be processed in that order.

In the same field of endeavor, Anderson clearly shows and discloses prioritizing messages based on their intended destination such that tasks received by different nodes can be processed simultaneously; (see abstract, "The packet prioritization station operates to give priority to transmissions to those destinations that have a higher number of associated origins.").

Therefore, it would have been obvious to a person of ordinary skills in the art at the time the invention was made to incorporate the prioritization packets based on destinations with higher priority as taught by Anderson to the data transferring system disclosed by Pettey as modified by Yasuda for purpose of sending data based on precedence of the receivers. The proper motivation is to organizing the transmitting data based on the receivers' priority.

However, Pettey as modified by Yasuda and further as modified by Anderson fail to disclose prioritizing messages intended for same nodes chronologically such that they can be processed in that order.

In the same field of endeavor, Ise discloses prioritizing messages intended for same nodes chronologically such that they can be processed in that order (lines 49-52 of col. 4 “a core node carries out a transfer processing with respect to received packets according to the priority level described in each received packet.”).

Therefore, it would have been obvious to a person of ordinary skills in the art at the time the invention was made to incorporate the method for process the prioritized received data packet as taught by Ise by the destinations disclosed Pettey as modified by Yasuda and further as modified by Anderson for purpose of handling the most important data in turn. The proper motivation is to process the received data based on their primacy.

9. **Claims 7 and 8** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Pettey et al. (U.S. Patent # 6,594,712 B1)** (hereafter Pettey) in view of **Anderson (U.S. Patent # 6,931,003 B2)** and further in view of **Ise et al. (U.S. Patent # 6,643,258 B1)** (hereafter Ise).

Consider **claim 1**, Pettey clearly shows and discloses a method for the communication of message packets between nodes in a data processing system, said method comprising the steps of:

establishing a first set of communication parameters prior to message transmission time in a communications adapter connected to a first one of said nodes, said first set of communication parameters including a destination identifier (see FIG. 9, FIG. 2 and lines 27-30 of col. 12, "a plurality of local address fields 912 to 918 for specifying addresses on the PCI buses 212 and 216 of FIG. 2." See FIG. 8 and lines 13-23 of col. 12 "The WQE 800 also includes a SGL local address field 812 for specifying the physical address in local memory 218 of a scatter/gather list (SGL), described below with respect to FIG. 9... The WQE 800 also includes other fields 816 for specifying information necessary... destination local ID, destination global ID..." and Lines 25 of col. 14, for utilizing SGLs 900 to generate the transmit packet by TxPP logic 1414 of FIG. 14);

establishing a second set of communication parameters prior to message transmission time in a communications adapter connected to a second one of said nodes, said second set of communication parameters including an entry which maps said destination identifier to an address in memory in said second node (see lines 43-45 for utilizing SGLs 900 of FIG. 9 by RxPP logic 1416 of FIG. 14, "The RxPP logic 1416 also utilizes SGLs 900 of FIG. 9 to transfer data in a received packet to local addresses on the PCI buses 212 and 216." See FIG. 5 for mapping memory and lines 45-49 of col. 14, "If the received packet is an RDMA ...then the local PCI addresses will be specified in the DRDMA Address Space 508 of FIG. 5.");

transmitting a message packet with header information linking said packet to said first and second set of communication parameters, whereby data in said packet is transferred directly from memory locations in said first node directly to memory locations in memory at said second node (see lines 28-30 of col. 1 for a direct memory accessing, "One feature of the IBA that facilitates high-speed data transfers is the Remote Direct Memory Access (RDMA) operation."; and lines 2-4 of col. 8 for creating IB packet headers; and FIG. 4 for format of a Packet Memory Block (PMB) and lines 64-67 of col. 8 for linking IB parameters in the PMB packets; IB are created for WQE which includes SGL as described in lines 32-34 of col. 11 and line 13 of col. 12);

However, Pettey fails to disclose prioritizing messages based on their intended destination such that tasks received by different nodes can be processed simultaneously; and prioritizing messages intended for same nodes chronologically such that they can be processed in that order.

In the same field of endeavor, Anderson clearly shows and discloses prioritizing messages based on their intended destination such that tasks received by different nodes can be processed simultaneously; (see abstract, "The packet prioritization station operates to give priority to transmissions to those destinations that have a higher number of associated origins.").

Therefore, it would have been obvious to a person of ordinary skills in the art at the time the invention was made to incorporate the prioritization packets based on destinations with higher priority as taught by Anderson to the data transferring system disclosed by Pettey for purpose of sending data based on precedence of the receivers. The proper motivation is to organizing the transmitting data based on the receivers' priority.

However, Pettey as modified by Anderson fail to disclose prioritizing messages intended for same nodes chronologically such that they can be processed in that order.

In the same field of endeavor, Ise discloses prioritizing messages intended for same nodes chronologically such that they can be processed in that order (lines 49-52 of col. 4 “a core node carries out a transfer processing with respect to received packets according to the priority level described in each received packet.”).

Therefore, it would have been obvious to a person of ordinary skills in the art at the time the invention was made to incorporate the method for process the prioritized received data packet as taught by Ise by the destinations disclosed Pettey as modified by Anderson for purpose of handling the most important data in turn. The proper motivation is to process the received data based on their primacy.

Consider **claim 8 as applied to claim 7 above**, In addition Ise discloses said tasks intended for same node are queued chronologically (lines 41-44 of column 8, “Note also that "priority control" used in the following description means a control to allocate communication resources for each class, and can be realized by a variety of mechanisms including strict priority queuing…”).

Allowable Subject Matter

10. **Claims 5-6, 9-10, 18-20** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Consider **claim 5**, the best prior art found during the examination of the present application, Pettey et al. (U.S. Pub. # 6,594,712 B1) fails to specifically disclose, teach or suggest a modified method of claim 4, the step of determining if said channel has any other tasks assigned to it.

Consider **claim 6**, the best prior art found during the examination of the present application, Pettey et al. (U.S. Pub. # 6,594,712 B1) fails to specifically disclose, teach or suggest a modified method of claim 4, if no other tasks are assigned to said channel, said packet is then dispatched and said channel is blocked until said task is completed and a signal is provided that a new task can be started.

Consider **claim 9**, the best prior art found during the examination of the present application, Ise et al. (U.S. Patent # 6,643,258 B1) fails to specifically disclose, teach or suggest a modified method of claim 8, the step of providing signals from one task to another such that when one task completes its processing another queued task begins processing immediately.

Consider **claim 18**, the best prior art found during the examination of the present application, Pettey et al. (U.S. Pub. # 6,594,712 B1) fails to specifically disclose, teach or suggest a modified method of claim 15, a specialized register is provided for at least one of said channels such that through said register, said channel can only be accessed by one task associated with said specific channel.

Consider **claim 20**, the best prior art found during the examination of the present application, Pettey et al. (U.S. Pub. # 6,594,712 B1) fails to specifically disclose, teach or suggest a modified method of claim 17, a specialized register is provided for each channel such that through said channel can be accessed through said register by only one task at one time that is associated with said channel.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to**:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Hand-delivered responses should be brought to

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

13. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Allahyar Kasraian whose telephone number is (571) 270-1772. The Examiner can normally be reached on Monday-Thursday from 8:00 a.m. to 5:00 p.m.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Rafael Pérez-Gutiérrez can be reached on (571) 272-7915. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or 571-272-4100.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist/customer service whose telephone number is (571) 272-2600.

Allahyar Kasraian
A.K./ak
November 7, 2007

Rafael Perez-Gutierrez
Supervisory Patent Examiner
Technology Center 2600
Art Unit 2617
11/7/07